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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,215	11/19/2003	Kenneth Stern	A2WI2320US	9062

23935 7590 02/07/2005

KOPPEL, JACOBS, PATRICK & HEYBL
555 ST. CHARLES DRIVE
SUITE 107
THOUSAND OAKS, CA 91360

EXAMINER	
LE, JOHN H	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,215	STERN, KENNETH	
	Examiner	Art Unit	
	John H Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) 1-25 are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-12, drawn to a method of autocalibrating a plurality of phase-delayed clock signal edges within a reference clock period.

II. Claims 13-22, drawn to an apparatus for measuring the time delay between adjacent clock edges.

III. Claims 23-24, drawn to a method of calibrating a timing vernier.

IV. Claim 25, drawn to an apparatus for measuring the time delay between adjacent phase-delayed clock edges.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case In the instant case, invention I has separate utility such as invention of group I does not required a variable delay module in said delay signal path, said delay cell having a delay bias input; and a phase detector having respective inputs coupled to said target and delay signal paths; wherein said variable delay module is operable to delay a first clock signal on said delay path so that a bias input signal presented to said delay bias input, when a bias input signal is present, corresponds to the time delay between said first clock signal and a second clock signal on said target signal path of group II and invention of group II does not required steps measuring delay

spacings between said plurality of clock signal edges; calculating desired delay spacings from said delay spacings; calculating ideal signal edges from said desired delay spacings of group I.

Inventions I and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as invention of group I does not required said phase-delayed clock signal edges dividing one period of a reference clock; comparing a vernier clock signal edge to one of said plurality of phase-delayed clock signal edges after said phase-delayed clock signal edges have been autocalibrated; adjusting said vernier clock signal edge to match said one phase-delayed clock signal edge; wherein said clock edge is calibrated and available for calibrated use by a user of group III and invention of group III does not required steps measuring delay spacings between said plurality of clock signal edges; calculating desired delay spacings from said delay spacings; calculating ideal signal edges from said desired delay spacings of group I. See MPEP § 806.05(d).

Inventions I and IV are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case In the instant case, invention I has separate utility such as invention of group I does not required means for comparing first and second clock signal edges, when said first and second clock signals are present, said means for

comparing connected to said phase-shifted clock signal lines; means for measuring delay spacing between said first and second clock signals, when said clock signals are present; and means for selectively adjusting said first clock signal to match said second clock signal, when said first and second clock signals are present of group IV and invention of group IV does not required steps measuring delay spacings between said plurality of clock signal edges; calculating desired delay spacings from said delay spacings; calculating ideal signal edges from said desired delay spacings of group I.

Inventions II and III are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case In the instant case, invention II has separate utility such as invention of group II does not required steps of autocalibrating a plurality phase-delayed clock signal edges to match respective ideal signal edges, said phase-delayed clock signal edges dividing one period of a reference clock; comparing a vernier clock signal edge to one of said plurality of phase-delayed clock signal edges after said phase-delayed clock signal edges have been autocalibrated; adjusting said vernier clock signal edge to match said one phase-delayed clock signal edge; wherein said clock edge is calibrated and available for calibrated use by a user of group III and invention of group III does not required a variable delay module in said delay signal path, said delay cell having a delay bias input; and a phase detector having respective inputs coupled to said target and delay signal paths; wherein said variable delay module is operable to delay a

first clock signal on said delay path so that a bias input signal presented to said delay bias input, when a bias input signal is present, corresponds to the time delay between said first clock signal and a second clock signal on said target signal path of group II.

Inventions II and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as invention of group II does not required means for comparing first and second clock signal edges, when said first and second clock signals are present, said means for comparing connected to said phase-shifted clock signal lines; means for measuring delay spacing between said first and second clock signals, when said clock signals are present; and means for selectively adjusting said first clock signal to match said second clock signal, when said first and second clock signals are present of group IV and invention of group IV does not required a variable delay module in said delay signal path, said delay cell having a delay bias input; and a phase detector having respective inputs coupled to said target and delay signal paths; wherein said variable delay module is operable to delay a first clock signal on said delay path so that a bias input signal presented to said delay bias input, when a bias input signal is present, corresponds to the time delay between said first clock signal and a second clock signal on said target signal path of group II. See MPEP § 806.05(d).

Inventions III and IV are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as

claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case In the instant case, invention IV has separate utility such as invention of group IVdoes not required steps of autocalibrating a plurality phase-delayed clock signal edges to match respective ideal signal edges, said phase-delayed clock signal edges dividing one period of a reference clock; comparing a vernier clock signal edge to one of said plurality of phase-delayed clock signal edges after said phase-delayed clock signal edges have been autocalibrated; adjusting said vernier clock signal edge to match said one phase-delayed clock signal edge; wherein said clock edge is calibrated and available for calibrated use by a user of group III and invention of group III does not required means for comparing first and second clock signal edges, when said first and second clock signals are present, said means for comparing connected to said phase-shifted clock signal lines; means for measuring delay spacing between said first and second clock signals, when said clock signals are present; and means for selectively adjusting said first clock signal to match said second clock signal, when said first and second clock signals are present of group IV.

A telephone call was made to James K. Dawson on 01/28/2005 to request an oral election to the above restriction requirement, but did not result in an election being made.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H Le whose telephone number is 571-272-2275. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John H. Le

Patent Examiner-Group 2863

January 28, 2005

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H Le whose telephone number is 571-272-2275. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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John H. Le

Patent Examiner-Group 2863

February 1, 2005